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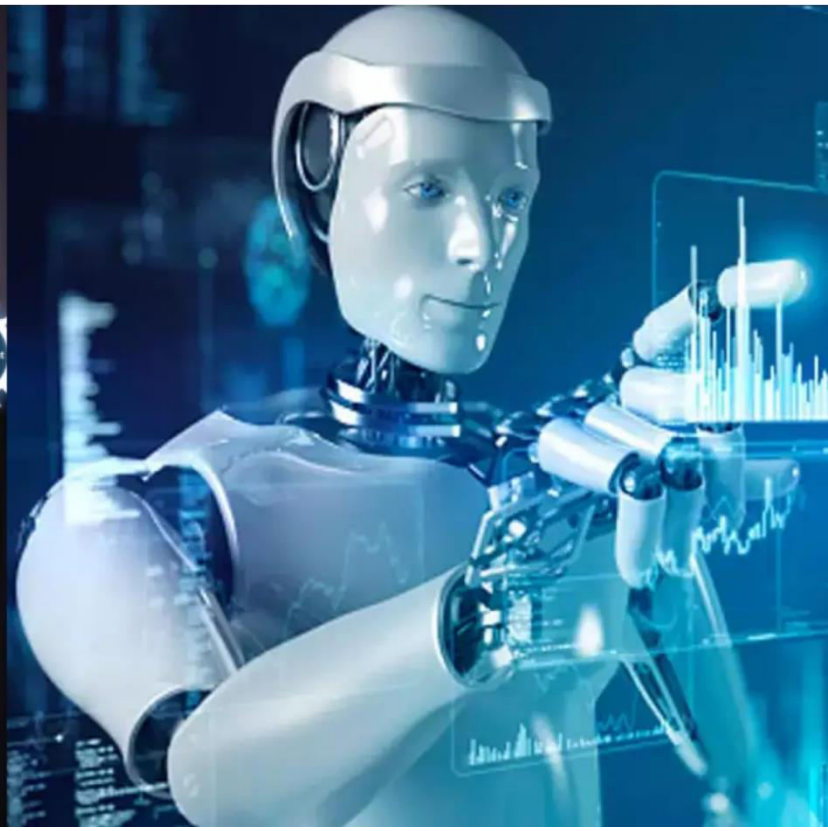

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High-Security Image Encryption using ANN-Driven Chua Chaotic Model in System Verilog

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ABSTRACT: In recent years, the rapid growth of digital communication and multimedia exchange has increased the need for secure transmission of image data. Conventional encryption techniques often face challenges such as limited key space, vulnerability to statistical attacks, and high computational complexity when applied to large image datasets. To address these issues, this work proposes a high-security image encryption and decryption system based on an Artificial Neural Network (ANN)-driven Chua chaotic model, implemented using SystemVerilog for hardware efficiency. The proposed system integrates the unpredictable behavior of Chua's chaotic system with the adaptive learning capability of ANN to generate highly complex and dynamic encryption keys. Initially, the input image is processed in MATLAB, where it is converted into a structured numerical format suitable for hardware-based processing. The ANN module optimizes the parameters of the chaotic system to enhance randomness and increase the overall security strength of the generated key stream. The encryption process is implemented using a SystemVerilog-based architecture, where pixel data is securely encrypted using chaotic sequences through bitwise operations. The design is validated using ModelSim simulation to ensure functional correctness and is synthesized using Xilinx tools for hardware implementation feasibility. The decrypted output is reconstructed in MATLAB using the inverse encryption process. Experimental evaluation shows that the proposed system provides strong resistance against cryptographic attacks, high key sensitivity, and accurate image reconstruction. The combination of ANN optimization, chaotic dynamics, and hardware-level implementation makes the system suitable for real-time secure image transmission applications in embedded systems and FPGA-based security platforms.

KEYWORDS: Image Encryption, Chua Chaotic System, Artificial Neural Network, SystemVerilog, FPGA, Cryptography, Hardware Security, Secure Communication.

I. INTRODUCTION

The rapid expansion of digital communication technologies has significantly increased the exchange of multimedia data across various platforms. Among different types of multimedia, images are widely used in applications such as medical diagnostics, military surveillance, online transactions, and social networking. As image data is highly sensitive and often transmitted over unsecured networks, ensuring its confidentiality and integrity has become a major concern. Traditional cryptographic algorithms such as AES and DES, although secure for textual data, may not always be efficient for image encryption due to the large data size, high redundancy, and strong correlation between adjacent pixels. To overcome these limitations, research has shifted toward alternative approaches such as chaos-based cryptography and intelligent optimization techniques. Chaotic systems are highly suitable for encryption due to their inherent properties like sensitivity to initial conditions, randomness, and ergodicity. Chua's chaotic circuit is one such nonlinear system that generates complex and unpredictable behavior, making it an effective candidate for secure key generation in encryption systems. However, the performance of chaotic systems depends heavily on system parameters, which must be carefully selected to ensure maximum randomness and security. In parallel, Artificial Neural Networks (ANNs) have gained attention for their ability to learn and optimize complex nonlinear relationships. By integrating ANN with chaotic systems, it becomes possible to dynamically optimize chaotic parameters, thereby improving the quality and unpredictability of encryption keys. This hybrid approach enhances both security strength and adaptability of the system. In this work, a hardware-efficient image encryption and decryption system is proposed using an ANN-driven Chua chaotic model implemented in SystemVerilog. The system leverages MATLAB for preprocessing and post-processing, while FPGA-oriented hardware design ensures real-time performance. The combination of chaos

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theory, neural network optimization, and hardware implementation provides a robust and scalable solution for secure image transmission in modern embedded and communication systems.

II. LITERATURE SURVEY

1. A Survey of Chaos-Based Image Encryption Algorithms
Author : S. Li and Y. Zhang
Year : 2020
Description :
This paper provides a comprehensive survey of chaos-based image encryption techniques, focusing on different chaotic maps and their applications in securing digital images. The authors analyze various chaotic systems such as Logistic map, Lorenz system, Chen system, and Chua's circuit, highlighting their effectiveness in generating pseudo-random sequences for encryption purposes. The study emphasizes that chaotic systems are highly suitable for image encryption due to their inherent properties such as sensitivity to initial conditions, ergodicity, and unpredictability. The paper explains how chaotic sequences are used to perform permutation and diffusion operations on image pixels, thereby breaking the correlation between adjacent pixels. It also compares different chaos-based encryption methods in terms of security strength, computational complexity, and implementation efficiency. The authors observe that although chaos-based systems offer high security, their performance depends heavily on parameter selection and system initialization, which can sometimes limit robustness. Additionally, the paper highlights the importance of hardware implementation for real-time applications, as software-based systems often suffer from latency issues. It concludes that chaos-based encryption remains a promising field for secure image transmission but requires further improvement in terms of optimization and hybrid integration with intelligent systems such as neural networks. This study provides a strong theoretical foundation for the proposed ANN-driven Chua chaotic encryption system, particularly in understanding how chaotic behavior can be leveraged for secure image processing.

2. FPGA Implementation of Real-Time Image Encryption Using Chaotic Maps
Author: A. Kumar and R. Singh
Year: 2020
Description:
This research paper focuses on the hardware implementation of image encryption systems using chaotic maps on FPGA platforms. The authors propose a real-time encryption architecture that leverages the Logistic chaotic map to generate encryption keys for secure image transmission. The study emphasizes the importance of hardware acceleration in cryptographic systems, especially when dealing with large image datasets that require fast processing. The proposed system is implemented using HDL and synthesized on FPGA to evaluate performance metrics such as speed, area utilization, and power consumption. The results demonstrate that FPGA-based implementations significantly outperform traditional software-based encryption systems in terms of processing speed and real-time capability. The chaotic map is used to generate pseudo-random sequences, which are then applied to pixel permutation and diffusion processes. The paper also discusses the limitations of using a single chaotic map, particularly regarding limited key space and vulnerability to certain cryptographic attacks if parameters are not carefully chosen. It suggests that hybrid approaches combining multiple chaotic systems or integrating optimization techniques could enhance security. Overall, the study highlights the effectiveness of FPGA-based encryption systems for real-time applications such as medical imaging and secure communications. It also provides valuable insights into hardware design considerations, which are directly relevant to the proposed SystemVerilog-based implementation. This work supports the idea that hardware acceleration is essential for achieving high-performance and secure image encryption systems.

III. METHODOLOGY

The methodology of the proposed image encryption system is structured into a sequence of well-defined stages that integrate MATLAB processing, ANN optimization, chaotic key generation, and SystemVerilog-based hardware implementation. The process begins with image acquisition, where the input image is imported into MATLAB and converted into a numerical pixel matrix. This matrix is normalized and reshaped into a one-dimensional stream to ensure compatibility with digital hardware design. In the next stage, an Artificial Neural Network (ANN) is employed to optimize the parameters of the Chua chaotic system. The ANN analyzes input conditions and adjusts chaotic parameters to maximize randomness, improve entropy, and enhance the unpredictability of the generated key sequence. This optimized configuration forms the basis of secure key generation. Following this, the Chua chaotic system

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generates a pseudo-random key stream based on nonlinear differential equations. The generated chaotic sequence is highly sensitive to initial conditions, ensuring strong security characteristics. This key stream is then used in the SystemVerilog encryption module, where pixel data is encrypted using bitwise XOR operations in a pipelined architecture for high-speed processing. The design is verified using ModelSim simulation to ensure correctness of encryption and decryption operations. Finally, FPGA synthesis is performed using Xilinx tools, and MATLAB is used for post-processing to reconstruct the decrypted image, confirming accurate and lossless recovery.

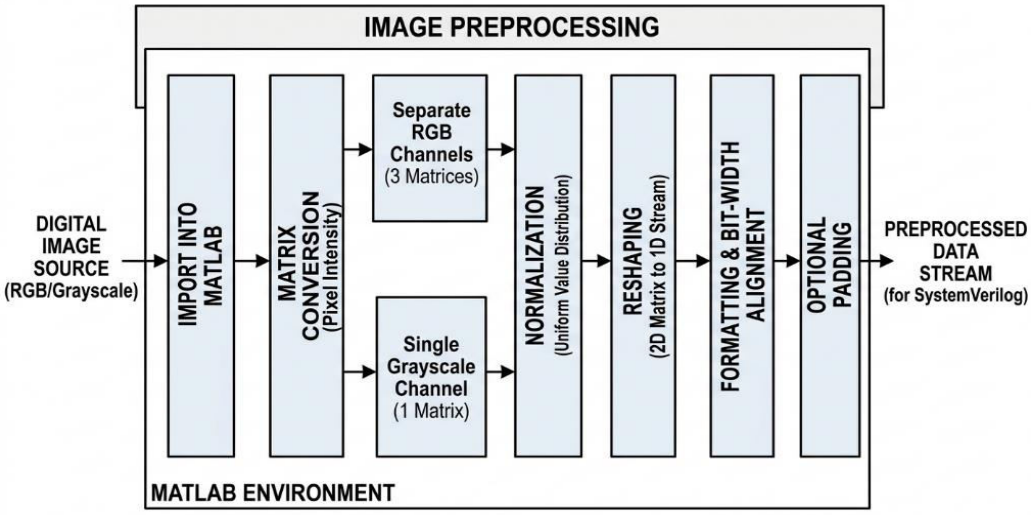

Figure 3.1.IMAGE PREPROCESSING

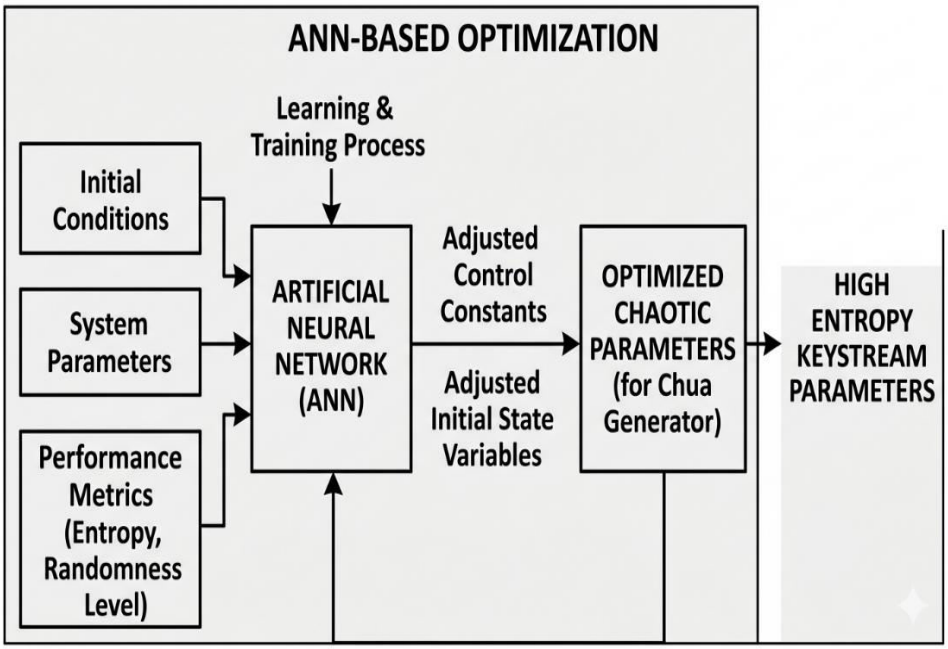

Figure.3.2. ANN-BASED OPTIMIZATION

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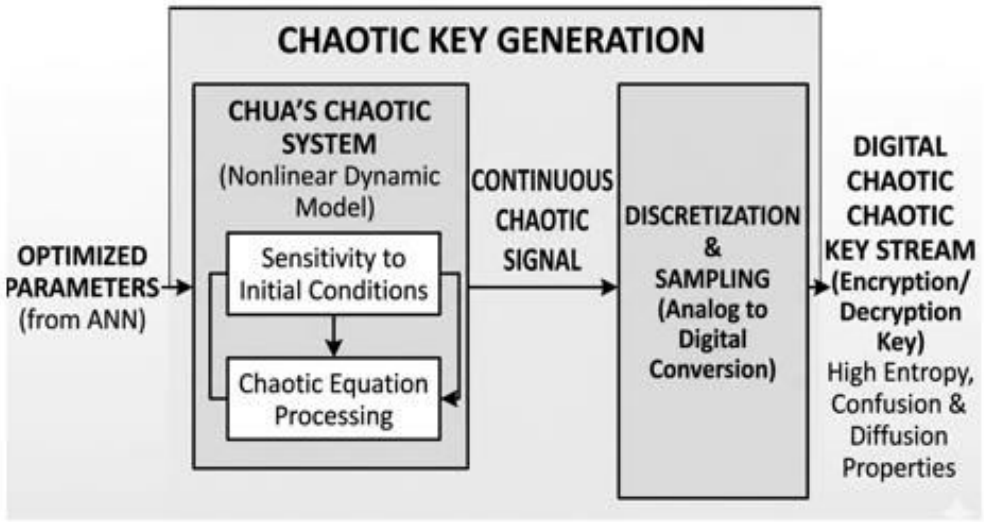

Figure.3.3. CHAOTIC KEY GENERATION

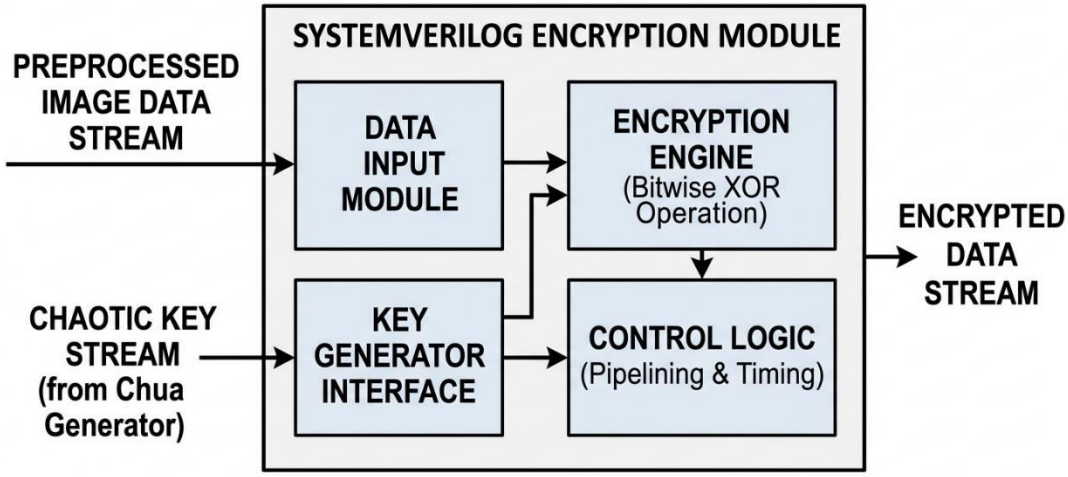

Figure.3.4 HARDWARE ENCRYPTION DESIGN

IV. EXPERIMENTAL RESULTS

SIMULATION RESULT

Verilog HDL is a Hardware Description Language (HDL). A Hardware Description Language is a language used to describe a digital system, for example, a computer or a component of a computer. One may describe a digital system at several levels. For example, an HDL might describe the layout of the wires, resistors and transistors on an Integrated Circuit (IC) chip, i. e., the switch level. Or, it might describe the logical gates and flip flops in a digital system, i. e., the gate level. An even higher level describes the registers and the transfers of vectors of information between registers. This is called the Register Transfer Level (RTL). Verilog supports all of these levels. However, this handout focuses on only the portions of Verilog which support the RTL level.

VERILOG:

Verilog is one of the two major Hardware Description Languages (HDL) used by hardware designers in industry and academia. VHDL is the other one. The industry is currently split on which is better. Many feel that Verilog is easier to learn and use than VHDL. As one hardware designer puts it, "I hope the competition uses VHDL." VHDL was made an

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IEEE Standard in 1987 and Verilog in 1995. Verilog is very C-like and liked by electrical and computer engineers as most learn the C language in college. VHDL is very most engineers have no experience. Verilog was introduced in 1985 by Gateway Design System Corporation, now a part of Cadence Design Systems, Inc.'s Systems Division. Until May, 1990, with the formation of Open Verilog International (OVI), Verilog HDL was a proprietary language of Cadence. Cadence was motivated to open the language to the Public Domain with the expectation that the market for Verilog HDL-related software products would grow more rapidly with broader acceptance of the language. Cadence realized that Verilog HDL users wanted other software and service companies to embrace the language and develop Verilog-supported design tools.

SIMULATION RESULTS

The simulation of the proposed ANN-driven Chua chaotic image encryption system was carried out using ModelSim to verify the functional correctness and performance of the SystemVerilog design. The main objective of the simulation was to ensure accurate encryption and decryption of image data, validate chaotic key generation, and observe the timing behavior of the hardware modules. Initially, the input pixel stream obtained from MATLAB preprocessing was applied to the encryption module. The chaotic key stream generated using the ANN-optimized Chua system was successfully synchronized with the pixel data. The encryption process demonstrated correct bitwise XOR operation, resulting in a completely randomized output that showed no visible correlation with the original image data.

***** SIMULATION RESULTS*****

The simulation model included modular blocks such as the chaotic key generator, encryption core, control unit, and decryption module. Each module was tested independently and then integrated to verify system-level functionality. The ModelSim environment allowed step-by-step observation of signal transitions, ensuring that data flow between modules was stable and synchronized. The simulation confirmed that ANN-optimized parameters correctly influenced the chaotic generator, producing highly random sequences suitable for encryption. The decrypted output was then validated by applying the inverse process using the same chaotic key stream. The reconstructed pixel stream matched the original input data without any loss or distortion, confirming lossless decryption.

***** WAVE FORMS*****

Waveform analysis provided detailed insight into the behavior of signals across different modules. The encryption waveforms clearly showed the transformation of input pixel values into encrypted outputs, while maintaining synchronization with the chaotic key signal. The decryption waveforms verified that applying the same key stream successfully restored the original pixel values. Timing analysis indicated that the system operates efficiently with minimal delay, making it suitable for real-time applications. Overall, the simulation results confirm that the proposed system is functionally correct, highly secure, and capable of efficient hardware-based image encryption and decryption.

V. CONCLUSION

CONCLUSION

The proposed work presents a high-security image encryption and decryption system based on an Artificial Neural Network (ANN)-driven Chua chaotic model implemented using SystemVerilog. The primary objective of enhancing image security in digital communication has been successfully achieved by integrating chaos theory, machine learning, and hardware design techniques into a unified framework. The system effectively addresses the limitations of conventional encryption algorithms, particularly in handling high redundancy and strong pixel correlation present in image data. The use of Chua's chaotic system ensures high randomness and sensitivity to initial conditions, which significantly strengthens the encryption process. Furthermore, the incorporation of ANN improves the overall performance by dynamically optimizing chaotic parameters, resulting in higher entropy and an expanded key space. This hybrid approach enhances resistance against various cryptographic attacks, including brute-force, statistical, and differential attacks. The hardware implementation using SystemVerilog ensures efficient processing with reduced latency, making the system suitable for real-time applications. Simulation using ModelSim confirms the functional correctness of both encryption and decryption modules, while FPGA synthesis using Xilinx tools validates the hardware feasibility of the proposed architecture. MATLAB-based preprocessing and post-processing further ensure accurate transformation and reconstruction of image data without loss. Experimental observations indicate that the proposed system achieves secure transmission, high-speed processing, and accurate image recovery. The combination of ANN, chaotic systems, and hardware acceleration provides a robust and scalable solution for modern secure communication systems. Overall, the proposed architecture demonstrates a significant improvement over traditional

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encryption techniques in terms of security strength, computational efficiency, and real-time performance capability, making it highly suitable for embedded and FPGA-based security applications in image communication systems.

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